Approaches to scalable quantum computing towards error correction with long ion chains



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What are the <u>key ingredients</u> required for a *useful* trapped-ion quantum computer?



SCALABLE ION TRAPS: DESIGN



5 silica glass wafers

- Ion-to-electrode distance 185 um
- Wafer machining precision: 1 um (xy),
- Dedicated zones: splitting, transport Junctions allow for

Top view



RF

RF

 $\Pi \Pi \Lambda$

JUNCTION OPTIMISATION

- TRANSPORT
- X-junction traps don't confine in the junction centre x
- A symmetry breaking is required, such as a connection between RF electrode
- A 'bridge' creates pseudopotential barriers which the ion needs to traverse
- Size and shape of the 'bridge' matters: we can optimize it for minimal heating during transport



Optimised bridges create low (0.02-0.05 eV) RF barriers while still confining at the centre (0.5-1MHz)

S. Ragg, C. Decaroli et al., Segmented ion-trap fabrication using high precision stacked wafers, Rev. Sci. Instr. 90 (2019)

SCALABLE ION TRAPS: IMPLEMENTATION







Grounded copper sleeve



- Trap and PCB inserted in copper sleeve
- Effusion Calcium oven for loading
- Helical resonator provides 200 V RF @ 35.5 MHz
- In cryostat @ 7K



Cryostat housing trap, resonator, oven, imaging lens and delivery optics

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INDIVIDUAL ION MANIPULATION

ADDRESSING

ADDRESSING: Pitch reducing fibre array

PROFA spatial schematic







• 11 cores with 5 um pitch

• 2um mode field diameter

- In cryostat, only 9mm from ions!
- Insensitive to trap vibrations
- Short paths mitigate phase noise
- Beam profile measured with an ion
- Side lobes indicate some core to core crosstalk
- Commercial device: improvements are possible



FIRST EXPERIMENTS IN A SCALABLE ION TRAP





OUTLOOK AND FUTURE EXPERIMENTS



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